Application Note

Application Note

AN1142

APM32F003x4x6 Application Note

Version: V1.0

1 Introduction

This application note provides precautions to be taken when using APM32F003x4 and APM32F003x6.

Contents

2 Note to Hardware Application Design

2.1 Design of MCU Filter Capacitor

The chip power ports (VDD, VSS) and VCAP pins need to be connected in parallel to large and small filter capacitors. The effectiveness of capacitors depends on the optimal placement and connection type. PCB layout requires star-shaped wiring, and it is important to note that the external power supply passes through large and small capacitors and then connects to the chip. The large and small filter capacitors should be placed as close to the chip as possible within 4mm. The reference is: BULK capacitor, CAP capacitor, and DEC decoupling capacitor are above 10uF, 2.2uF, and 100nF, respectively.

Note: In low-temperature applications, the actual capacitance value of the capacitor may decrease. It is recommended to connect a 105 capacitor (1uF) at the Vcap port. Connecting a small capacitor may cause the chip to fail to work normally.

Figure 1 TSSOP20 and SOP20

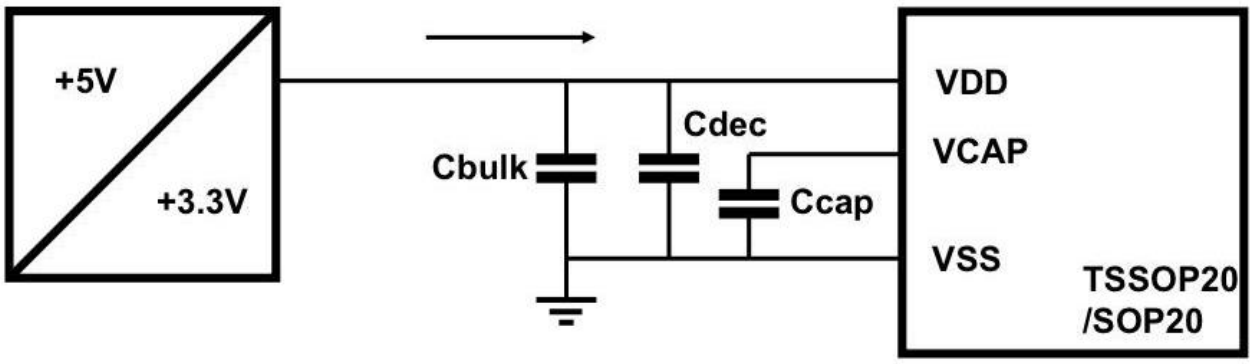
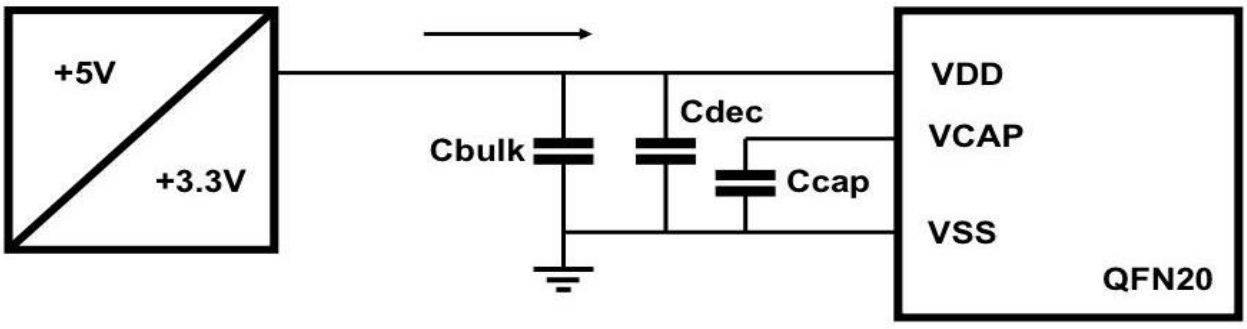


Figure 2 QFN20

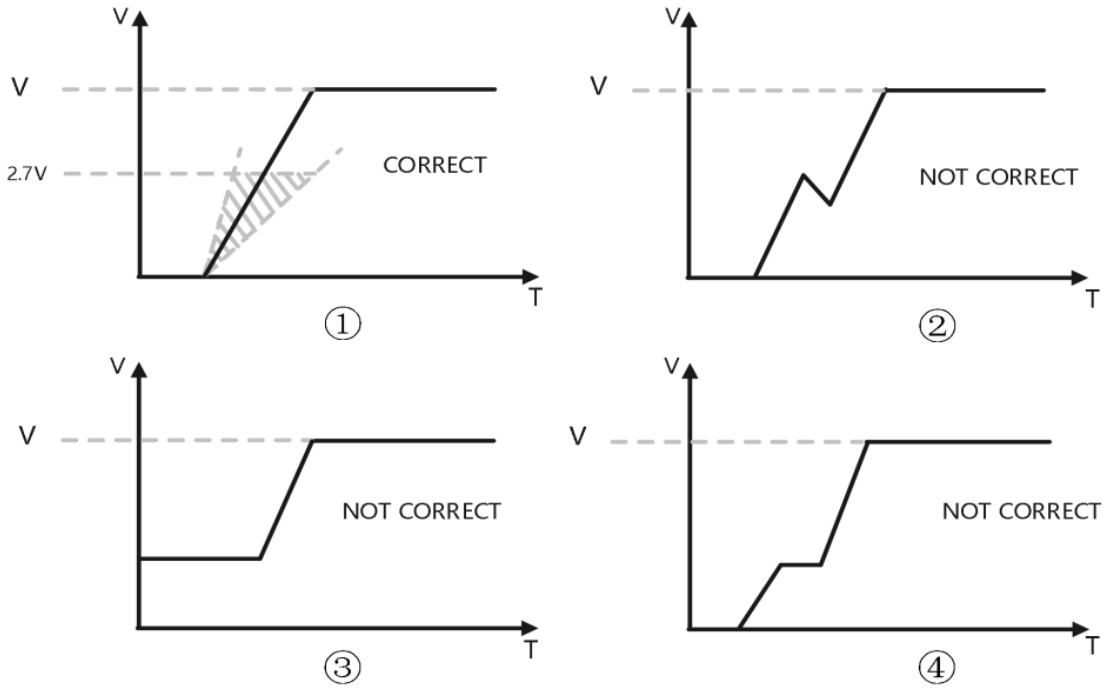


2.2 Precautions for MCU Power Supply

The MCU's power supply ramp rate should meet the maximum and minimum value limits specified in the datasheet, namely greater than 0.5V/min and less than 100V/ms respectively. It takes at least 55us to increase from 0V to 5.5V, and at least 24us to increase from 0V to 2.4V. Too high or too low power-on rate may cause the MCU to fail to work normally; MCU needs to be

powered down to below 300mV before being powered on again, and the above time must meet the requirements within the full temperature range. The power-on startup waveform needs to meet the waveform ① in Figure 3, while the other three waveforms are incorrect.

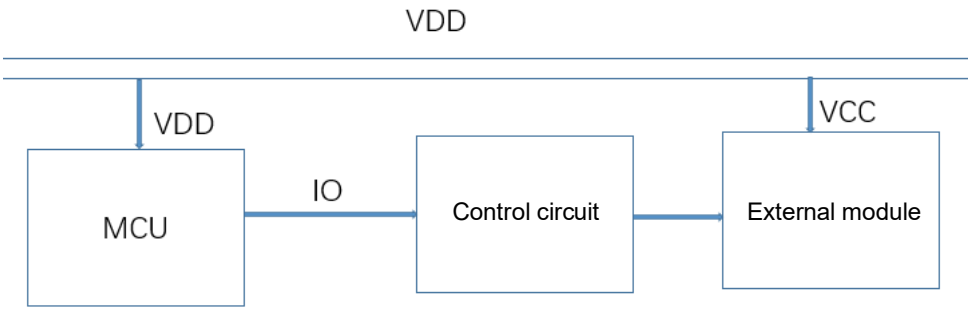
Figure 3 Power-on Waveform



2.3 The peripheral module uses VDD and VSS

When MCU is used to control the power supply or power-on process of external modules, too high power-on rate should be avoided to prevent the problem of VDD voltage being pulled down due to sudden current changes. To ensure stable operation of the system and protect the circuit from potential damage, it is recommended to adopt appropriate delay measures for steady power supply conversion. The power-on speed can be adjusted by adding appropriate buffer elements, such as capacitors or resistors, so that voltage dip will not be caused to VDD due to instantaneous high current demand. If sudden dip is caused for this reason, the drop speed must also meet the requirements of the ECU's power supply ramp rate. (Use examples shown in Figures 4 and 5)

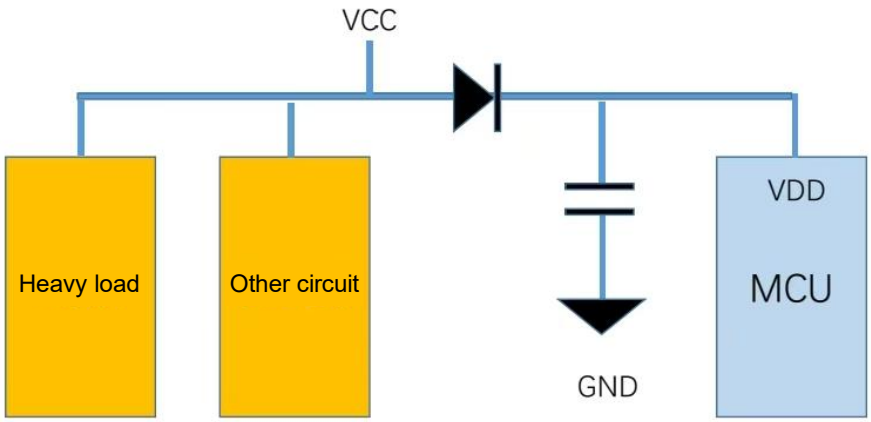
Figure 4 IO Control Peripheral Module



In order to avoid power fluctuation, in applications where MCU power supply is above 3.6V, connect a low voltage-drop diode in series on the circuit or connect a 10R resistor in series and a capacitor of above 10uF in parallel to form a fast power drop protection circuit. If the capacitance is large enough, the power down will be slow and the power-down magnitude can be very small.

Note: If the germanium diode conducts, there will be a voltage drop of 0.2V, which will reduce the power supply of the MCU by 0.2V compared to before. If ADC is used, the accuracy may be affected.

Figure 5 Shared Power Supply for Peripherals



2.4 External and High-frequency Signals

- Attention should be paid to checking whether an instantaneous increase in load may be caused by zero-crossing signals, relay signals, AC loads, etc. The load impact can be mitigated by bypass capacitors.
- For high-frequency IIC clock lines, high-frequency SPI clock lines, etc., it is important to check whether instantaneous peak currents will be generated.
- When controlling the LDO to connect the back-stage power supply to the circuit, add a 300uF large capacitor or delay circuit to the LDO backend circuit to prevent sudden drop in supply voltage and MCU reset when connecting LDO.

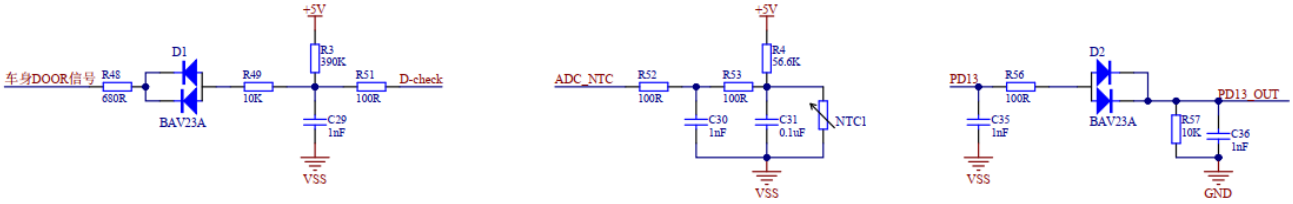
2.5 Connect the Input/Output signal port to a current limiting resistor in series and connect the capacitor to VSS in parallel

For Input/Output ports (e.g. ADC, external interrupts, communication interfaces, etc.), it is recommended to connect to the protective resistors in series in circuit design. The resistance value should be considered and calculated, and the theoretical maximum current should not exceed the limit parameters that the chip port can withstand; the resistors connected in series and capacitors connected in parallel should be placed as close as possible to the chip pins, and the resistors should be connected in series before the capacitors are connected in parallel. The ground of the filter capacitor of the peripheral module must be connected to the ground that has

passed through the large and small filter capacitors (VDD, VSS). As shown in Figure 6, the IO port is connected in series to a 100R resistor and connected in parallel to a 1nF capacitor.

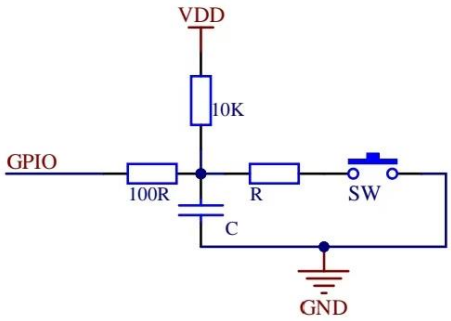
Note that in the design of PCB interconnection (similar to separating lamps from control modules, separating sensors from control modules), this series-connected resistors and parallel-connected capacitors should be placed on the PCB board of the chip. Reasonable parameters and placement positions can effectively prevent damage to the chip ports by ESD/EOS.

Figure 6 An Example of Resistor and Capacitor Connection



For button circuits, the recommendations are as follows:

Figure 7 Button Circuit



It is recommended to use a 220nF capacitor for C in Figure 7, and a small resistor R, e.g. 1k or 100R, can be connected in series next to the button. At the same time, the capacitor C should be placed close to the button SW when drawing the drawing boards. So that it can avoid the negative impact pressure generated by buttons.

2.6 When using IO as the input terminal of the sensor, connect a capacitor of 1MΩ or above to pull down

Different pins of the same PORT can only be configured with the same external trigger interrupt. When the IO port reads a pulse, it is easy to interfere with other IO ports and generate interrupt count. Connect a resistor of 1MΩ or above to the sensor input port to pull down and stabilize the IO port level at a fixed level, in order to avoid false triggering or repeated counting of interrupts.

2.7 IO voltage cannot be higher than VDD voltage

When the IC is not powered by VDD, but there is voltage at the IO port, this voltage will be supplied to the IC through a pull-up protection diode. Or when the IC is powered by VDD, but

there is a higher voltage at the IO port than VDD, the voltage difference between this voltage and VDD will cause the pull-up protection diode to conduct, making the current flow into VDD. Under normal circumstances, IO cannot exceed 0.3V above VDD.

This phenomenon can easily cause the following hazards:

(1) Too high current will cause the clamp diode on the IO port to quickly overload and be damaged.

(2) It will make MCU reset unsuccessfully.

(3) It will cause disorder in the chip program.

(4) A latch-up effect will result.

2.8 Pay Attention to Protection for Exposed Ports

- For communication ports, ESD protection measures are required. A small resistor 100R can be connected in series on the signal line to limit the amplitude of ESD current; transient voltage suppressor diodes (TVS) can be connected in parallel on the signal line, near the interface position.
- There is a hot-plugging risk in the burning port, and it should be protected by first contacting GND and then contacting IO during the connection.
- The reset pin should be connected to an external capacitor, but it should not be too large, which may cause the pin to not be fully pulled down and result in abnormal burning. So it is recommended to connect the capacitor to 100nF.

3 Precautions for Software Application

3.1 Precautions for GPIO Operation

1. Unused GPIO ports should be set to output low level or connect an external 100Ω resistor for pull-down.

2. Different GPIO pins should avoid being configured with the same multiplexing function!

3. When the chip VDD is powered on within the range of 0V-2.4V, the GPIO port is in an uncertain state, and attention should be paid to the impact of unstable condition of GPIO on the stability of the post-stage drive circuit; when VDD is powered on above 2.4V, after the chip completes the power-on reset, the status of the GPIO port will be executed according to the program settings.

4. If the input state is maintained when PA1 enters sleep mode, the state will be pulled down. If there are applications where PA1 maintains pulled up in sleep mode, the PA1 port should be configured as output before entering sleep mode.

5. The conflict between the main function configuration and interrupt configuration of GPIO should be avoided. Variables can be used as mutex flags for evasion or only serve as flags in interrupt functions, and the assigned value of GPIO is executed in the main while task.

For example: continuously configuring PD3 in the while of the main program, enabling timed interrupts, flipping PD3 during interrupt, and encountering PD3 flipping exception after running.

3.2 Precautions for ADC Configuration

In the single-channel continuous conversion mode, before configuring CSR in ADC1_ConversionConfig library function, first configure the bit continuous scan mode; otherwise, EOC cannot be set when initializing the second channel, and ADC cannot be used.

The specific steps are:
(1) Configure continuous scan mode;
(2) Configure CSR;
(3) Normally configure continuous or discontinuous mode;
(4) Enable the scan mode.

3.3 Precautions for SPI Configuration

In the application of SPI, when the host restarts during communication, as the cache data is not transmitted completely, the TXBEF of the slave is empty, but there is still other data in the transmit cache, and continuing the communication at this time will cause communication failure.

When modifying operating parameters of SPI, it is necessary to reset the SPI clock and reconfigure it. If the parameters are initialized directly, communication will fail.

3.4 Precautions for USART and TMR Configuration

1. When using PB4 and PB5 as input and output pins of serial ports, as these two pins only have open- drain outputs, they need to connect to a pull-up resistor to be used together.

2. The following two application scenarios should be avoided:

If USART2 is turned on, TMR1A_CH1 (PD1) will fail to output PWM;
If USART3 is turned on, TMR2_CH3 (PA3) will fail to output PWM.

3.5 Precautions for Low-power Mode Operation

In applications that require repeated wake-up, it should avoid entering low-power mode in interrupt service functions, which may make the chip fail to wake up repeatedly.

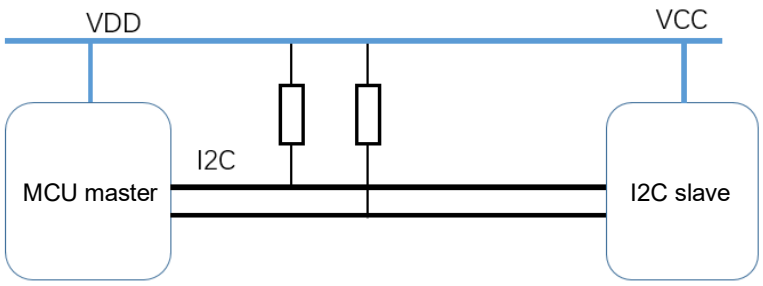
3.6 Precautions for I2C

In the process of sudden power failure and recovery of pull-up power supply of SCL/SDA, there is a possibility that the combination of SCL/SDA voltage and logic timing may trigger START but not STOP, resulting in the bus remaining in BUSY state. Recommended avoidance scheme:

1. The pull-up power supply of I2C must be stable to prevent the power supply from dropping too low due to instability during use. For common scenarios of I2C master-slave communication, the following hardware design is recommended:

a. The host and slave share power supply;

Figure 8 I2C Communication Circuit



b. When the host and slave cannot share power supply, it is recommended to connect the power supply of pull-up resistor to the power supply of host MCU.

2. The bus can also be released by resetting the slave. If EEPROM is used as a slave, it is impossible to reset the salve using the software, and the bus release function needs to be added to the I2C host when establishing a new communication. Due to the probability of bus locking, the bus BUSY status timeout function can be added. Combination of the two can improve the robustness of the system.

3. If the I2C device on the bus can recognize power failure, turn off the I2C module before power failure.

4 Precautions for Use of Simulators/Burning Tools

4.1 The development environment supports IAR and KEIL

1. IAR is recommended to use V8.50.5 version and above.

2. KEIL is recommended to use MDK-ARM V5.36 version.

Note: For the projects that fail to compile with a low-version MDK cannot be used after it has been updated to a higher version, the original error project cannot be used, and the SDK program needs to be decompressed again for use.

3. J-Link software is recommended to use 7.96o version and above.

4.2 Compilation and Burning

1. The APM32 ROG V1.014 burner upper computer released on Geehy's official website should be used to cooperate with OB.

F003 is easy to enter a self-locking state when debugging and burning through JLink or ST-LINK.
Usually, users will operate OB themselves in the main function, and if the OB operation is interrupted or incomplete, the chip will be locked easily because there are configuration bits for read protection and write protection on the OB address. In addition, abnormal changes in the OB value may also lead to abnormal program operation or system crash.

2. ST-LINK only supports SWD communication in the 3.3V power domain. When it is powered by 5V, it may fail to connect and identify the chip. Therefore, it is recommended that 3.3V external power supply should be used and switched to ST-LINK direct power supply or the SWD pin should be connected to an external pull-up resistor during burning and debugging.

3. When the burning software does not provide the part number of APM32F003, the part number of M0 or M0+ core can be selected for burning or J-FLASH can be used.

5 Revision history

Table 1 Document Revision History

Date	Version	Revision History
January,2025	1.0	New

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